31st Year *1986-2017*

ADVANCE PROGRAM

BCTM 2017
31st Annual IEEE BIPOLAR / BiCMOS CIRCUITS AND TECHNOLOGY MEETING

Miami Marriott Biscayne Bay
Miami, FL, USA

October 19 - 21, 2017
SHORT COURSE - October 21, 2017

SPONSORED BY

THE ELECTRON DEVICES SOCIETY OF THE INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS

IN COOPERATION WITH

THE IEEE SOLID - STATE CIRCUITS SOCIETY
THE IEEE MICROWAVE THEORY & TECHNIQUES SOCIETY

Conference Website: http://ieee-bctm.org

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2017 BCTM SCHEDULE AT A GLANCE		
Thursday - October 19		
Registration opens at 7:30 AM - ***Bayview Foyer (2nd Floor)****Conference **Boardroom*** **- Attendee Lounge Opens at 8:00 am**		
8:30AM - 9:00 AM	Welcome and Announcements ***Bayview Ballroom***	
9:00AM - 10:00AM	Keynote speaker : Prof. Zhenqiang (Jack) Ma (Univ of Wisconsin) At the Horizon of Wide Bandgap Bipolar Junction Transistors: The Viability of Lattice Mismatched Heterojunctions ***BayvView Ballroom***	
10:00AM - 10:20AM	Coffee Break ***BayvView Ballroom***	
10:20AM - 12:00PM	**1**. Low Power Analog and Linearization ***Bayview Ballroom***	**2**. Device Physics for Advanced Applications ***Watson Island***
12:00PM - 1:15PM	**Lunch Break** ***(Self – Arrangement)***	
1:15PM - 2:35PM	**3.** Emerging Technologies ***Bayview Ballroom***	
2:35PM - 2:55PM	Coffee Break	
2:55PM - 5:00PM	**4.** Advanced Transceivers ***Bayview Ballroom***	**5.** Advanced SiGe BiCMOS Process Modules ***Watson Island***
5:00PM - 6:00 PM	Break	
6:00 PM - 10:00 PM	**Dinner Cruise:** Boarding is at 6:00 PM directly in back of the Marriott Biscayne Bay, we will return back to the hotel at 10:00 PM.	

Friday - October 20		
Registration opens at 8:00 AM - ***Bayview Foyer (2nd Floor)***		
8:30AM - 9:30AM	Keynote speaker : Prof. Albert Wang (Univ of California, Riverside) Advances in ESD Protection Designs: A Dino to Dash ***Bayview Ballroom***	
9:30AM - 9:50AM	Coffee Break	
9:50AM - 11:30AM	**6.** Beamforming and Receiver Circuits ***Bayview Ballroom***	**7.** Lost in Modeling? **Watson Island**
11:30AM - 1:00PM	**Lunch Break** ***(Self – Arrangement)***	
1:00PM - 2:40PM	**8.** Optical Communications Circuits ***Bayview Ballroom***	**9.** Boosting Device Performance **Watson Island**
2:40PM - 3:00PM	Coffee Break	
3:00PM - 5:05PM	**10**. Conversion Circuits ***Bayview Ballroom***	**11**. Millimeter-Wave VCOs and Signal Generation ***Watson Island***

Saturday - October 21	
SHORT COURSE ONLY Registration & Breakfast at 7:30 AM ***Bayview Foyer (2nd Floor) Conference Boardroom*** *- Attendee Lounge Opens at 8:30am*	
8:30AM - 5:10PM	**SHORT COURSE - Saturday, October 21** ***SiGe HBT device modeling and circuit design*** ***Watson Island***
5:10 PM	**END OF BCTM 2017 - - - THANK YOU FOR ATTENDING!**

31st Year *1986-2017*

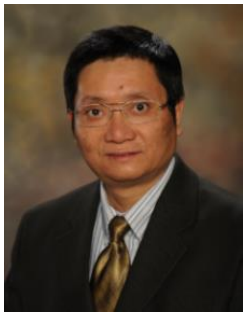
Welcome from the BCTM 2017 Chairmen

Welcome to the beautiful Miami! On behalf of the IEEE BCTM Executive Committee, we are honored and delighted to present the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) 2017.

Conference highlights:

- Keynote addresses from world-renowned speakers:
  - Discussion Topic/Speaker: “Large Lattice-Mismatched Heterojunctions Through UO-Interfaced Material Grafting for Wide Bandgap Bipolar Junction Transistors” by Ma Zhenqiang of the University of Wisconsin–Madison
  - Discussion Topic/Speaker: “Advances in ESD Protection Designs: A Dino to Dash” by Albert Wang of University of California–Riverside ”
- Full-day short course:
  - Discussion Topics/Speakers: “SiGe HBT device physics and modeling” by Professor M. Schröter from Technical University Dresden and “Circuit Design in SiGe-BiCMOS for High-Frequency and High-Speed Applications” by Professor J.R. Long from University of Waterloo
- Forward-looking Emerging Technologies Session with two invited speakers:
  - Discussion Topics/Speakers: “High resolution terahertz gas spectroscopy with a SiGe BiCMOS transmitter and receiver” by Professor Heinz-Wilhelm Hübers (Institut für Planetenforschung, DLR) and “Silicon-Germanium heterostructures for quantum computing” by G. Scappucci (QuTech and Kavli Institute of Nanoscience, TU Delft
- Invited papers exploring advances in analog and wireless design, device physics, modeling and simulation, and process technology.
- Technical papers covering the latest advances in physics, design, performance, fabrication, characterization, modeling, and application of Si/SiGe/SiGe:C bipolar, and BiCMOS ICs
- A fabulous evening banquet dinner and boat cruise around Miami.

The IEEE BCTM is the world’s premier forum focused on the needs and interests of the bipolar and BiCMOS community. If you are interested in leading edge bipolar/BiCMOS devices and technology, circuits, and applications, as well as networking with experts in these areas, please kindly join us this year in historic Miami, Florida, USA!



Foster Dai
General Chair
Auburn University

Peter Magnee
Technical Program Chair
NXP

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BCTM 2017 REGISTRATION

Click here to register http://ieee-bctm.org

Advance registration deadline is Thursday, September 7, 2017.

Registration Fees: MAIN MEETING (October 19-20)
Group Registration rates are available for Companies and Organizations sending 5 or more participants to BCTM 2017. Please contact cshaw.cmpevents@gmail.com for more details.

(1) Conference Registration Cost in US Dollars (includes conference program, USB proceedings, banquet cruise, and all day refreshments.

	ADVANCE (By 9/7/2017)	REGULAR (Starting 9/8/2017)
IEEE Members	$675	$775
Non-Members	$775	$875
Students	$500	$500

(2) Guest Fee for Dinner Banquet

	$115/person	$125/person

(3) Extra 2017 Proceedings (electronic version on USB drive):

IEEE Members	$50
Non-Members	$75

Registration Fees: SHORT COURSE (October 21)
(1) Course Cost (includes lunch):

Members	$400	$400
Non-Members	$400	$400
Students	$300	$300

Notes:
*All fees are denominated in US$
*Full Registration for the conference Includes: USB, continental breakfast, all day refreshments, and banquet cruise. Lunch is on your own. *Short Course Registration includes: course notes/USB, continental breakfast, lunch, refreshments

Refund/Cancellation Policy:
All requests for refund/cancellation must be received in writing at least 10 days prior to the conference start date for a full refund on or before September 28, 2017. Any requests thereafter will not be entitled to a refund. Cancellations will incur a $50 USD administration fee. Please submit cancellation requests via email to cshaw.cmpevents@gmail.com.

HOTEL RESERVATIONS

A block of rooms has been reserved at special discounted rates for BCTM conference participants at our host hotel below. While there are alternatives, we would like to remind attendees to please support the conference and fully enjoy all the activities by staying at the official host hotel. The Symposium relies on attendees staying at the conference hotel. Room reservations should be made as soon as possible before the hotel cut-off date below, as there are a limited number available at the group rate.

MIAMI MARRIOTT BISCAYNE BAY
1633 North Bayshore Drive
Miami, Florida 33132 USA
T: +1 305-374–3900
Website

Click here to Book your Hotel Room

Check-in Time: 4:00 PM Check-out Time: 12:00 PM

1 Restaurant, 1 café, 2 bars
Fitness center
Outdoor pool
On-site water and land activities
Nearby golf & spa

Hotel Accommodations

- **Room Reservation**: You are responsible for booking your hotel room at the conference hotel. **Click here** to reserve your room or call reservations at 1-800-228-9290 or (305) 374-3900. You must reference BCTM when making your reservation. Room, tax, and incidentals will be billed to the credit card you provide.**Guest Room Rate**: Single $179.00 plus tax (13%)
  An extra person charge per person may apply for 2 or more guests sharing the same guestroom. The Group Rate will be provided 3 days before and after meeting dates (October 19-21, 2017), based on availability.
- **Reservation Cut-Off Date**: Reservations must be made by the cut-off date, Tuesday, September 19 by 5:00 PM EST in order to receive the group rate and guarantee availability. After this date, rooms will be on a space available basis and at possibly higher rates. We recommend you book early.
- **Changes or Cancellations**: Contact the hotel directly.

Internet & Parking

- Discounted internet in guestrooms will be provided to IEEE guests at $5.00 per room, per night. Marriott Rewards Members will receive complimentary internet in guestrooms. Complimentary Wi-Fi is available in the lobby and public areas.
- Parking is available on property.
  On-site Parking Fee: $29 USD daily
  Valet Parking Fee: $34 USD daily

TRAVEL ARRANGEMENTS

Air Travel

- You are responsible for booking your own air travel.
- Airport Options: The Miami International Airport (MIA) is about 9 miles or 20 minutes from the Miami Marriott Biscayne Bay Hotel. The Fort Lauderdale International Airport (FLL) is about 28 miles or 56 minutes from the hotel. Both airports accommodate domestic and international travel.
- Special Airfares: Travel arrangements using the IEEE negotiated air carriers or the carriers of your choice can be made through World Travel, Inc.
    - Call in: Between 8:00 AM and 5:30 PM EST Monday through Friday. Within the US and Canada, call (800) TRY-IEEE, +1 800 879-4333); and outside of the US and Canada, call +1 717 556-1100.
    - Online: Visit their website at http://www.ieee.org/travel.
    - Email: Email your request to ieee@worldtravelinc.com.
- Departure: On October 21, you will need to book airline reservations no earlier than 3:30pm to allow ample travel time to Miami International Airport. Travel time to the airport is approximately 12 minutes from the hotel.

Ground Transportation

- Uber: ~$18-$45 one way (MIA) or ~$50-$100 one way (FLL)
- Lift: ~$18-$45 one way (MIA) or ~$50-$100 one way (FLL)
- Miami Shuttle Van: ~$15 one way (MIA) or ~$50 one way (FLL)
- Taxi: ~$26 one way (MIA) or ~$80 one way (FLL)
- Car Service: 305-898-4315 https://drivenmiami.com
- Discounted Car Rentals: IEEE corporate car rental discounts are available to all attendees. Use discount codes here when calling your preferred car rental company to receive special rates: Avis A606000, Budget X520000, Hertz 61368, and Enterprise NA24IE1.
- Driving Directions from the Miami International Airport (MIA):
  Take 836 E. to 395 (Miami Beach) Exit.
  Exit to Biscayne Blvd, turn left onto Biscayne Blvd.
  Turn right on NE 14th Street.
  Go 1 block, turn left onto North Bayshore Drive. Hotel is on the right side of street at 1633 N. Bayshore Dr.
- Driving Directions from the Fort Lauderdale Airport (FLL):
  Take I-95 South to 395 East to Biscayne Blvd exit.
  Turn left onto Biscayne Blvd. Take a right turn on NE 14th Street.
  Go one block to N. Bayshore Drive and make a left turn onto N. Bayshore Drive. The hotel is on the right side of street at 1633 North Bayshore Drive.

ADDITIONAL INFORMATION

CONFERENCE BANQUET: Thursday, October 19, 2017:
BCTM's 2017 final banquet will take place onboard the **"Biscayne Lady Yacht"** a premiere Miami charter cruise. Attendees will enjoy amazing views of South Florida's emerald waters, celebrity homes and more. Attendees will also enjoy luxury, comfort, and flavorful menu items in addition to an experience of a lifetime! Boarding is at 6:00 PM directly in back of the Marriott Biscayne Bay. We will return back to the hotel at 10:00 PM sharp!

ADMISSION All interested persons are welcome to register and attend the BCTM; you do not have to be an IEEE member. Admission to sessions requires a BCTM badge. Please wear your badge at all times.

REGISTRATION Complete registration information is contained in the centerfold of this booklet as well as on the conference's web page (http://ieee-bctm.org/). Please use the website to register. The advanced registration deadline is **September 7, 2017**. All conference activities are included in the registration fees (technical sessions, food breaks and the banquet) as well as a USB flash drive with an electronic copy of BCTM 2017 Proceedings.

OTHER CONFERENCE SOCIAL EVENTS Several events have been arranged to promote informal social interactions among conference participants.

TUTORIAL / SURVEY TALKS Tutorial talks given by invited experts are intended to give a broad overview of a given subject with a critical review of technology and applications. They are twice the length of the usual contributed talk with longer abstracts in the Proceedings.

MEMBERS OF THE PRESS: You are welcome to attend BCTM. Admission is free. Just present your business card at the registration desk.

RECRUITING Intensive recruiting undermines the purposes for which the BCTM was established, and is contrary to IEEE policy.

BEST STUDENT PAPER AND BEST PAPER AWARDS BCTM offers a Best Paper Award. The BCTM Best Paper Award recognizes and promotes high quality contributions to scholarly research among professionals who author and present papers at the conference. All papers submitted in non-student category are eligible for consideration for the Best Paper Award.

The BCTM Best Student Paper Award recognizes and promotes outstanding research led by students. To be eligible for consideration for the Best Student Paper Award, the following criteria have to be met: 1) the student must have carried out a substantial part of the research reported in the paper, 2) the student must be the first author and must present the paper at the conference, 3) the paper must be identified as a student paper during submission of the paper; and 4) the paper identified as a student paper in submission, but not presented by the student will be disqualified for Best Student Paper Award competition. In this scenario, the paper will be moved to non - student category for Best Paper Award competition automatically.

Eligible papers are evaluated by the Best Paper Award Committee and the notifications will be sent out after the conference. The winners of the awards will be recognized with a $500 check and a plaque at next year's BCTM conference.

FURTHER INFORMATION BCTM is sponsored by the IEEE Electron Devices Society (EDS) in co - operation with the IEEE Solid - State Circuits Society (SSCS) and the IEEE Microwave Theory & Techniques Society (MTT).

BCTM 2017 Short Course and Schedule

Watson Island

Date: Saturday, October 21, 2017
Time: 7:30 AM - 5:10 PM
Discussion Topic: Bipolar Transistor Device Physics and Circuit Design Primer
Speakers:

- Circuit Design: Professor John Long, U. Waterloo, Ontario, Canada
- Device Physics: Professor Michael Schröter, TU Dresden, Germany

7:30 - 8:30 AM Registration and breakfast

8:30 - 8:40 AM Welcome

Michael Schroter and Laleh Najafizadeh

Course Overview

The BCTM primer course will consist of two parts. The first part will present HBT device physics and establish the basis for the second part, which covers the design of basic high - frequency (HF) building blocks. Simple application examples will be common to both parts, thus providing a feel for device and circuit interaction.

8:40 - 9:40 AM

SiGe HBT device physics and modeling (I)

Instructor: Prof. M. Schröter (Technical University Dresden, Germany & UC San Diego, La Jolla, USA)

Based on a device performance comparison, the HBT modeling primer will start with the motivation why HBTs are and will remain a suitable choice for HF circuits. A brief overview on SiGe and III - V HBT device technology and the resulting device structures will precede the discussion on the basic operation principle of BJTs and HBTs These considerations will be based on the 1D transistor structure which determines the fundamental device behavior and nonlinearity. The explanation of the most relevant physical effects and their impact on currents and charges will be supported by 1D device simulation (TCAD) results using a sample doping profile. The discussion will also include non - quasi - static effects and noise correlation, which are typically considered second - order effects but can become important in HF circuits. Equipped with a working 1D model of a HBT, next the theory of the base resistance under different operating conditions and the modeling of emitter perimeter injection will be presented. Modeling of the realistic (3D) transistor structure will be completed by considering the various (parasitic) effects such as external series resistances, junction capacitances, substrate transistor and its HF coupling as well as self - heating and thermal coupling. Special emphasis will be put on geometry scaling with emitter dimensions and device configuration. The modeling results will be summarized in an equivalent circuit and related to existing compact models. Finally, simple application examples will be provided as a link to circuit design, showing the impact of certain transistor and geometry parameters on circuit performance.

Michael Schröter received his Dr. - Ing. degree (1988) and venia - legendi (1994) in electrical engineering from Ruhr - University Bochum, Germany. He held engineering and management positions at Nortel/BNR in Ottawa, Canada, and at Rockwell and RFNano Corp. in Newport Beach, CA, USA. Since 1999, he has been a Full Professor at Technical University Dresden, Germany. He is also Research Professor at UC San Diego and a co - founder of XMOD Technologies in Bordeaux, France, and has been leading the Carbon Path project within the German Excellence Cluster cfaed. He was the Technical Project Manager for the EU projects DOTFIVE and DOTSEVEN and is presently a member of the ITRS/IRDS RFAMS subcommittee, the BCTM and the CSICS TPC. He has co - authored over 200 publications and one

textbook.

9:40 - 9:55 AM Break

9:55 - 10:55 AM
SiGe HBT device physics and modeling (II)
Instructor: Prof. M. Schröter (Technical University Dresden, Germany & UC San Diego, La Jolla, USA)

10:55 - 11:10 AM Break

11:10 AM - 12:10 PM
SiGe HBT device physics and modeling (III)
Instructor: Prof. M. Schröter (Technical University Dresden, Germany & UC San Diego, La Jolla, USA)

12:10 - 1:30 PM Lunch

1:30 - 2:30 PM

Circuit Design in SiGe - BiCMOS for High - Frequency and High - Speed Applications (I)
Instructor: Prof. J.R. Long (University of Waterloo, Canada)

The design of high - frequency and high - speed front - end circuits is described in this course. A review of circuit benchmarks illustrates the relevance of device metrics (e.g., fT, fMAX) to circuit design goals. A series of examples are presented and analyzed in detail, including: low - noise preamplifiers, wideband amplifiers, voltage - controlled oscillators (VCOs and DCOs), and power amplifier drivers. System - level and circuit - level specifications for these sub - blocks are related in the context of current RF and high - speed applications. The use of passive components in the design and optimization of these circuits is also highlighted. Demonstrators illustrating the advantages offered by scalable models applied to the design of low - noise and power amplifiers will tie the content of this is lecture to the companion short course on device modelling. Finally, ESD protection of high - speed and high - frequency I/Os will be outlined.

John R. Long received the B.Sc. from the University of Calgary in 1984, and the M. Eng. and Ph.D. degrees in Electronics Engineering from Carleton University, Ottawa ON, in 1992 and 1996, respectively. He has worked at Bell - Northern Research Ltd., Ottawa, Canada, the University of Toronto (1996 - 2001), the Delft University of Technology in the Netherlands (2002 - 2014). In January 2015 he joined the ECE Department at the University of Waterloo in Canada. Professor Long's current research interests include: low - power transceiver circuitry for highly - integrated radio applications, and electronics design for high - speed data communication.

2:30 - 2:45 PM Break

2:45 - 3:45 PM

Circuit Design in SiGe - BiCMOS for High - Frequency and High - Speed Applications (II)
Instructor: Prof. J.R. Long (University of Waterloo, Canada)

3:45 - 4:00 PM Break

4:00 - 5:00 PM

Circuit Design in SiGe - BiCMOS for High - Frequency and High - Speed Applications (III)
Instructor: Prof. J.R. Long (University of Waterloo, Canada)

5:00 - 5:10 PM Course Evaluation

INTRODUCTORY REMARKS ND KEYNOTE

WELCOME AND ANNOUNCEMENTS

8:30 - 9:00 AM - ***Bay View Ballroom***

KEYNOTE SPEECH

9:00 - 10:00 AM - *Bay View Ballroom*

"At the Horizon of Wide Bandgap Bipolar Junction Transistors: The Viability of Lattice Mismatched Heterojunctions"

Prof. Zhenqiang (Jack) Ma (University of Wisconsin)

Research on heterojunction bipolar transistors (HBT) employing narrow bandgap semiconductors (e.g., Si/SiGe, GaInP/GaAs and InAlAs/InGaAs) have been mature and field-effect transistors employing wide bandgap semiconductors (e.g., GaN) have been well-developed. However, bipolar transistors employing wide bandgap semiconductors have faced severe technical challenges and no significant progress has been made within the last decades. The technical difficulties of creating bipolar transistors using wide bandgap semiconductors lie in the fact that all these wide bandgap semiconductors of interest (e.g., GaN, AlxGa1-xN, AlN, SiC, □-Ga2O3 and diamond) have either only good n-type or only good p-type doping, but not both. To overcome the doping challenges, two major approaches have been attempted for many years. One of them is to improve the doping quality of the poor doping type using growth methods. Regardless of some progress to increase carrier concentration, the approach has so far showed very limited promise for bipolar transistor applications. As for the other method, replacing the poorly doped wide bandgap material using other materials that are of the good doping type through various material bonding techniques has never led to satisfactory interfaces. Instead, the high density of states that served as a large amount of charge traps at the interfaces formed using such an approach have always resulted in non-ideal junction behavior, such as high ideality factor and high reverse leakage current in pn diodes formed thereof. In this keynote talk, I will first review the long history of extensive efforts of improving doping effectiveness through material growth and that of wafer bonding for making heterojunctions and diodes, and identify the insurmountable roadblocks of the two major approaches. Based on the review, I will detail our unique approach (US Patent: 8,866,154) in forming arbitrary large lattice-mismatched heterojunctions using ultra-thin foreign interfacial layers (e.g., UO and/or UN) that are able to repeatedly and reliably deliver ideal diode behavior with ideality factors in the range of 1.03-1.14 and an extremely low reverse leakage current density. Material analyses will be illustrated to understand the heterojunction formation mechanisms. I will also present various diodes that were experimentally formed between large lattice-mismatched single crystal semiconductors, such as Si/Ge, Si/GaAs, Si/GaN, GaAs/SiC, GaAs/GaN, Si/C and Ge/C, and several types of high-performance heterojunction bipolar transistors using the approach at University of Wisconsin-Madison over the last seven years to display the great promise of the heterojunction approach. Future perspectives of heterojunction bipolar transistors employing wide bandgap semiconductors will be exhibited.

Zhenqiang (Jack) Ma received his B.S. degree in applied physics and B.E. degree in electrical engineering from Tsinghua University in Beijing, China in 1991. He received his M.S. degree in nuclear science and M.S.E. degree in electrical engineering from the University of Michigan, Ann Arbor in 1997, and the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor in 2001. From 2001-2002, he was a member of the R&D team at Conexant Systems and later its spin-off, Jazz Semiconductor (now TowerJazz), in Newport Beach, CA. In 2002, he left Jazz to join the faculty of University of Wisconsin–Madison as an

assistant professor in the Department of Electrical and Computer Engineering. He is now a Lynn H. Matthias Professor in Engineering and a Vilas Distinguished Achievement Professor with affiliated appointments in four other departments and institutes in engineering and medical schools. His current interdisciplinary research covers (a) electrical engineering, including rigid, flexible, and stretchable high-speed electronics, optoelectronics and nanophotonics, and device physics, (b) materials science and engineering, including large lattice-mismatched arbitrary heterojunctions, semiconductor physics and semiconductor materials processing, (c) biomedical engineering, including brain-machine interfaces, synthetic neuronal circuits, optogenetics, genomics, and biomimetics, (d) energy, including power conversion devices, solar cells, and light emitting devices, (e) health, including implantable photoreceptor arrays for the visually impaired, and (f) engineering physics, including sensors for next-generation nuclear reactors and for spent fuel monitoring. He is the author or co-author of over 480 peer-reviewed technical papers and book chapters related to his research and holds 36 US and international patents or pending. His research innovations have attracted substantial attention from the media worldwide. He is a recipient of many awards including the Presidential Early Career Award for Scientists and Engineers (PECASE) bestowed upon by former President George W. Bush. As an individual well-versed in a wide breadth of topics, Zhenqiang Ma serves on the editorial boards, as an editor and technical reviewer of 83 international journals.

CONFERENCE PROGRAM

1. Low Power Analog and Linearization

Thursday 10:20 AM - Bay View Ballroom
Session Chair: Sorin Voinigescu
Co-chair: Patrice Gamand

(1.1) 10:20 AM - 11:10 AM - Ultra Low Power Analog Design and Technology for Artificial Neurons (Invited)
Francois Danneville
In a context of the end of Moore's law, energy dissipation constitutes a real challenge. Among the new energy efficient paradigms for data processing, bio-inspired computing is very promising, moreover introducing cognitive characteristics. As applications at very high scale are addressed, the size and energy dissipation of both the neuron and synapse cells needs to be minimized. In this context, this paper presents the design of an original artificial neuron, using standard 65nm CMOS technology with optimized energy efficiency and its application in basic neural networks. By recalling brain and neuron features, it is shown why neuron energy efficiency is roughly limited to 1 pJ/spike in biological neuron. Biological and artificial neurons features are carefully compared, highlighting the importance of downscaling. The artificial neuron circuit presented was designed to exhibit wide band spiking frequencies, targeting large scale bio-inspired information processing applications. The most important feature of the fabricated circuits is the neuron energy efficiency in the few fJ/spike range, which improves prior state-of-the-art by two to three orders of magnitude. This performance is achieved by minimizing two key parameters: the supply voltage and the related membrane capacitance. Meanwhile, the obtained standby power at a resting output does not exceed tens of picowatts. The circuit is sized to 35µm2, reaching a spiking output frequency of 26kHz. It is then shown how this artificial technology has already been used for two applications: (i) emulation of bursting mode, important in brain stimulation context or for robotics (locomotion rhythm), (ii) stochastic resonance application, useful to detect an electrical signal buried in noise, phenomena exploited in nature by species. These results already allow envisioning the development of highly integrated neuro-processors (vision applications). A variant circuit (biomimetic) could be used for robotics, neuroscience or medical applications.

(1.2) 11:10 AM - 11:35 AM - Training of Digital Predistortion Based on Signal-to-Distortion-Ratio Measurements

Jeffrey Lee, Ramon Gomez, and Sudhakar Pamarti
A novel training technique for digital predistortion (DPD) systems is presented. Previous techniques rely on the time-domain (TD) difference between the ideal transmitter input and the distorted amplifier output as an error metric. This work presents DPD training based solely on frequency-domain signal-to-distortion-ratio (SDR) information. The only a priori information required is the spectral occupancy of the desired signal. The approach is applied to a broadband SiGe BiCMOS power amplifier, including measured results.

(1.3) 11:35 AM - 12:00 PM - A Linearization Technique for Bipolar Amplifiers based on Derivative Superposition
Marco D'Avino, Jordi vd Meulen, Satoshi Malotaux, Marco Pelk, Michel Groenewegen, Paul Mattheijssen, Mark vd Heijden, and Leo de Vreede
A linearization technique for bipolar amplifiers based on Derivative Superposition is presented. The proposed technique provides excellent linearity, while having low sensitivity on the bias conditions. A demonstrator circuit, along with a reference circuit using out-of-band linearization for linearity comparison, have been designed and implemented in a 0:25µm SiGe:C BiCMOS technology to show the effectiveness of the proposed approach. Measured results show a significant IM3 improvement up to compression compared to the reference circuit.

2. Device Physics for Advanced Applications

Thursday 10:20 AM - Watson Island
Session Chair: Tomislav Suligoj
Co-chair: Jonggook Kim

(2.1) 10:20 AM - 10:45 AM - Operation of SiGe HBTs at Cryogenic Temperatures
Holger Rücker, Julian Korn, and Jens Schmidt
The operation of SiGe HBTs at cryogenic temperatures is investigated experimentally and theoretically. It is demonstrated that the collector current at cryogenic temperatures is caused by electron tunneling through the base. The temperature dependence of the transistor characteristics reveals a transition from conventional thermally activated transport at room temperature to tunneling dominated transport at cryogenic temperatures. Experimental results are presented for HBTs with a peak current gain of 8000 at 300 K and 45000 at 10 K.

(2.2) 10:45 AM - 11:10 AM - Thin-Film Layers with Interfaces that reduce RF Losses on High-Resistivity Silicon Substrates
Lis Nanver, Serge Evseev, Silvana Milosavljevic, and Lis Nanver
Radio-Frequency (RF) losses on High-Resistivity Silicon (HRS) substrates were studied for several different surface passivation layers comprising thin-films of SiC, SiN and SiO2. In many combinations, losses from conductive surface channels were reduced and increasing the number of interfaces between thin-films was found to be beneficial. In some cases the surface losses were completely eliminated. For example, with plasma-enhanced chemical-vapor deposition (PECVD) □-SiC layers up to a few tens of nm thick and exposed to nitridation or SiN growth at 850°. to form a SiC:N interface layer, values for the total losses of 1.6 dB/cm were achieved. Analysis of these layers was performed by using temperature dependent measurements of the RF losses on Coplanar Waveguides (CPWs), the capacitance-voltage characteristics and the sheet resistance along the Si surface. The overall results can be explained by assuming that the thin-films are so defected that they allow vertical current paths to highly-resistive interface layers where both fixed and mobile charge can be stored.

(2.3) 11:10 AM - 12:00 PM - CMOS beyond Si: Nanometer-Scale III-V MOSFETs (Invited)
Jesus del Alamo, Xiaowei Cai, Jianqiang Lin, Wenjie Lu, Alon Vardi, and Xin Zhao
CMOS electronics constitutes the backbone of our information society. The extraordinary success of CMOS is based on the unique scaling properties of the Si MOSFET. Over the last decade, increasing concerns have been expressed about the ability of the Si MOSFET to continue its

historical scaling path. This threatens the future of Moore's Law and its trifecta of benefits: cost, power and performance. For about a decade now, III-V compound semiconductors have been under intensive research in an effort to push Moore's Law beyond the point that Si can reach. How far have we come in this quest? This paper summarizes the state of the art of III-V compound semiconductor MOSFETs for future CMOS.

3. Emerging Technologies

Thursday 1:15 PM - Bay View Ballroom
Session Chair: Wibo van Noort

(3.1) 1:15 PM - 1:55 PM - High resolution terahertz gas spectroscopy with a SiGe BiCMOS transmitter and receiver (Invited)
Heinz-Wilhelm Hübers, Nick Rothbart, Klaus Schmalz, Johannes Borngräber, Selahattin Berk Yelmaz, and Dietmar Kissinger
High-resolution terahertz spectroscopy is a powerful tool for the identification of many gases due to their specific rotational transitions in that spectral range. Among the possible applications are the analysis of exhaled human breath that contains thousands of volatile organic compounds (VOCs) and the detection and identification of toxic industrial chemicals. The unique fingerprint spectra of these gases make a THz gas sensor very specific and sensitive. We present a THz spectroscopic system based on a gas absorption cell, a transmitter (TX) - and a receiver (RX)-module. The integrated TX and RX are fabricated in IHP's 0.13µm SiGe BiCMOS technology. We demonstrate TXs and RXs with integrated antennas for spectroscopy at 238 - 252 GHz and 495 - 497 GHz. The performance of the spectrometers will be presented and the potential for sensing applications will be discussed.

(3.2) 1:55 PM - 2:35 PM - Silicon-Germanium heterostructures for quantum computation (Invited)
Giordano Scappucci, D. Sabbagh, L. Yeoh, A. Sammak, M. Lodari, J. Boter, N. Kalhor, D. Brousse, M. Veldhorst, L. M.K. Vandersypen, N. Thomas, J. Roberts, R. Pillarisetty, P. Amin, H. C. George, K J Singh, and J S Clarke
Quantum computation is the man on the moon goal of the current second quantum revolution, in which quantum matter is engineered to develop disruptive technologies beyond the reach of classical understanding. How will we get there? In this talk I will discuss how we are turning everyday silicon into the quantum computing wonder material. Silicon-germanium heterostructures are a promising material stack for the development of spin qubits in silicon. To deploy a qubit into high volume manufacturing in a quantum computer requires stringent control over substrate uniformity and quality. Electron mobility and valley splitting are two key electrical metrics of substrate quality relevant for qubits. Here we present low-temperature magnetotransport measurements of strained Si quantum wells fabricated on 300 mm wafers within the framework of advanced semiconductor manufacturing. To ensure rapid progress in quantum wells quality we have implemented fast feedback loops from materials growth, to innovative heterostructure FET fabrication, and low temperature characterisation. In this direction we show recent progress in developing a cryogenic platform for high-throughput magnetotransport measurements.

4. Advanced Transceivers

Thursday 2:55 PM - Bay View Ballroom
Session Chair: Brian Floyd
Co-chair: Michael McPartlin

(4.1) 2:55 PM - 3:45 PM - Towards Energy-Efficient 5G Mm-Wave Links: Exploiting Broadband Mm-Wave Doherty Power Amplifier and Multi-Feed Antenna with Direct On-Antenna Power Combining (Invited)
Hua Wang
It is envisioned that future 5G wireless links will extensively employ multiple mm-Wave spectra (e.g., 28GHz, 37GHz, 39GHz, and 70GHz). A major bottom neck for silicon-based mm-Wave electronics lies in the generation of mm-Wave signals with high energy efficiency, high

linearity, and large modulation bandwidth, all of which are indispensable to support Gbit/s complex modulations with large peak-to-average-power ratio (PAPR) in 5G systems. In this paper, we focus on two technical aspects that recently attract increasing attention and may together address these challenges. We will first present Doherty power amplifier (PA) architecture that offers large back-off efficiency enhancement, linear operation, and low overhead on signal processing. A recent multi-band (28/37/39GHz) mm-Wave Doherty PA in a 130nm SiGe process will be presented as a design example. Next, we will present a new concept of antenna-electronics co-design at mmWave. A new "Multi-Feed Antenna" (MFA) is recently proposed and demonstrated by the authors to achieve direct on-antenna low-loss power combining of multiple mm-Wave PAs. A 60GHz all-silicon transmitter design employs on-chip MFA to combine power from 16 PAs and achieves state-of-the-art total radiated output power per transmitter element.

(4.2) 3:45 PM - 4:10 PM - A Multimode 5-6 GHz SiGe BiCMOS PA Design Powers Emerging Wireless LAN Radio Standards
Chun-Wen Paul Huang, Kenny Christainsen, Lui Lam, Andrew Chen, Mark Doherty, Mike McPartlin, and Bill Vaillancourt
A multimode 5-6 GHz SiGe BiCMOS PA IC that powers the emerging Wireless LAN applications is presented. The design can be realized in a 1.35 x 0.7 active area as a standalone power amplifier (PA) or the transmit (Tx) chain of a Front-end IC. The design features multiple modes with low DEVM supporting 1024 QAM data rates and >20 dB accurate power controls. The linearity is well scaled with supply voltage from 2.8V to 5.5 V and insensitive to modulation bandwidths and duty cycles. With a 5 V supply, the PA has 32 dB gain and meets -41 dB DEVM for 1024 QAM, up to 20 dBm Pout and -35 dB DEVM for 256 QAM 802.11ac up to 21 dBm Pout. The design has the also supports a low power mode having 3 dB less linear power, with reduced current. With DPD, the low linearity mode can achieve similar linear power as the high linearity mode with 40 mA current reduction. The diverse features of the PA IC simplify front-end circuit designs of emerging high throughput radio standards.

(4.3) 4:10 PM - 4:35 PM - 60GHz Concurrent Dual-Polarization RX Front-End in SiGe with Antenna-IC Co-Integration
Yao Liu and Arun Natarajan
Achieving a wideband, efficient, scalable and low-cost interface between IC and antennas is critical for mm-wave transceivers in silicon. This paper presents an antenna-IC co-integration approach to achieve dual-polarization transmission and reception using on-chip dual-pol feeds that aperture-couple through a slot in the on-chip ground to a patch antenna on the back side of the IC. The proposed wafer-scale compatible approach is demonstrated with a 60 GHz prototype that includes a dual-pol 60 GHz receiver frontend (RXFE) implemented in the TowerJazz SBC18H3 SiGe technology. The RXFE includes a cross-pol cancellation path (with variable gain and phase shift) to cancel cross-polarization leakage signal to enable concurrent dual-pol operation. The antenna co-integration approach achieves ~ 50% and 2.7 dBi simulated efficiency and gain, with measured dual-pol reception and ~30 dB cross-pol leakage cancellation. Extensive ground-plane reuse leads to the 60 GHz dual-pol RXFE and antenna feed and slot structures occupying 1.8 mm x 1.8 mm of die area.

(4.4) 4:35 PM - 5:00 PM - A novel compact balanced reflect-type vector modulator topology
Filipe Tabarani and Hermann Schumacher
A novel balanced reflect-type vector modulator topology is presented. The use of only four 90º hybrid couplers allows a much-reduced area, competitive with active solutions, while keeping all benefits of the passive topology. A test circuit was developed using a 0.25 µm SiGe BiCMOS technology. The K-band vector modulator occupies 353 x 435 µm and measurements showed a very well centered and uniformly distributed constellation. The maximum gain at 20.35 GHz equals -9.61 dB and return losses are above 10 dB. The use as a 16-QAM modulator is evaluated and in a 20% relative bandwidth, the circuit demonstrated amplitude and phase RMS errors of 0.7 dB and 4º, respectively.

Between the 16 configurations, the worst input referred 1dB compression point (Pin,1dB) obtained is 5.8 dBm with relative phase variations smaller than 3.73º.

5. Advanced SiGe BiCMOS Process Modules

Thursday 2:55 PM - Watson Island
Session Chair: Holger Rucker
Co-chair: Hiroshi Yasuda

(5.1) 2:55 PM - 3:20 PM - Performance Improvement of a Monolithically Integrated C-Band Receiver Enabled by an Advanced Photonic BiCMOS Process
Stefan Lischke, Dieter Knoll, Mohamed Hussein Eissa, Ahmed Awny, Marcel Kroh, Anna Peczek, and Lars Zimmermann
A monolithically integrated C-band receiver is used to demonstrate the potential of an advanced photonic BiCMOS process. We show that the particular SiGe HBTs integrated in this process strongly improve the receiver's frequency response, BER and noise behavior, compared to the same circuit fabricated in a previous process generation featuring slower transistors.

(5.2) 3:20 PM - 3:45 PM - 240 GHz RF-MEMS Switch in a 0.13 µm SiGe BiCMOS Technology
Selin Tolunay Wipf, Alexander Göritz, Christian Wipf, Matthias Wietstruck, Abdurrahman Burak, Eşref Türkmen, Yaşar Gürbüz, and Mehmet Kaynak
This paper presents an RF-MEMS switch fabricated in a 0.13 µm SiGe BiCMOS process technology for 240 GHz applications. The fabricated RF-MEMS switch provides a high capacitance Con/Coff ratio of 8.78 and beyond state of the art RF performances, 0.44 dB of insertion loss and 24.6 dB of isolation at 240 GHz. The return loss is better than 9.6 dB over the J-band (220 - 325 GHz). To the best of the authors' knowledge, the results achieved in this study are the lowest insertion loss and the highest isolation of a Single-Pole Single-Throw (SPST) switch reported at 240 GHz.

(5.3) 3:45 PM - 4:10 PM - SiGe HBT / CMOS Process Thermal Budget Co-optimization in a 55-nm CMOS Node
Alexis Gauthier, Pascal Chevalier, Gregory Avenier, Guillaume Ribes, Marie Lise Rellier, Yves Campidelli, Remi Beneyton, Didier Celi, Gerard Haury, and Christophe Gaquiere
This paper deals with the reduction of the process thermal budget in a 55-nm BiCMOS technology in order to improve the transit frequency of SiGe HBTs. Since MOSFETs are directly impacted by this modification, process adjustments are implemented to recover performance and parametric yield. The reduction of the spike annealing temperature, thermal oxidation replacement and Dynamic Surface Annealing implementation are discussed. A 355 GHz fT / fMAX HBT compatible with current 55-nm MOSFET models is demonstrated.

(5.4) 4:10 PM - 5:00 PM - 0.13-µm SiGe BiCMOS Technology with More-than-Moore Modules (Invited)
Mehmet Kaynak, Matthias Wietstruck, Alexander Goritz, Selin Tolunay Wipf, Mesut Inac, Barbaros Cetindogan, Christian Wipf, and Canan Baristiran Kaynak
This paper presents three different technology modules, integrated into a 0.13-µm SiGe BiCMOS process; namely RF-MEMS switch, microfluidics and heterogeneous integration technologies. The RF-MEMS switch module is optimized for mm-wave applications and offers superior performance figures at D-band with a wafer level encapsulated packaging option. The microfluidics module which is embedded by bonding three different wafers, provides a unique platform of fluid-electronic interaction with possibility of optical observation. Finally, the FOWLP option provides the heterogeneous integration of a single or multi chips in a single package. The BiCMOS process together with the integration of all these modules offers a technology platform to follow the More-than-Moore path for multi-functional and smart systems.

Friday, October 20, 2017

KEYNOTE SPEECH

8:30 - 9:30 AM - *Bay View Ballroom*

"Advances in ESD Protection Designs: A Dino to Dash"

Prof. Albert Wang (University of California, Riverside)

Electrostatic discharge (ESD) failure is a devastating IC reliability problem. Recent advances in IC technologies and designs, e.g., sub-28 CMOS, FinFET, 3D IC integration, power electronics, multi-core SoC and 5G RF ICs, makes on-chip ESD protection design extremely challenging. For decades, vast efforts have been devoted to research and development in ESD protection designs. This talk will give a historical review on ESD protection designs including the past, the current and the future. The talk will cover the ESD protection basics and fundamentals, current ESD protection design and ESD-IC co-design techniques, existing ESD protection solutions, emerging full-chip ESD design verification CAD methods, and future ESD protection concepts. As semiconductor technologies continue to advance and IC complexity rapidly increases, the dinosaur of ESD protection must dash to facilitate the future ICs.

Albert Wang received the BSEE degree from Tsinghua University and the PhD EE degree from State University of New York at Buffalo in 1985 and 1996, respectively. From 1995 to 1998, he was with National Semiconductor Corporation. From 1998 to 2007, He was a Professor of Electrical and Computer Engineering at the Illinois Institute of Technology. Since 2007, He has been a Professor of Electrical and Computer Engineering at the University of California, Riverside, where he is Director for the Laboratory for Integrated Circuits and Systems, Director for the University of California Center for Ubiquitous Communications by Light (UC-Light), and co-Director for SMIC-UCR-PKU Joint Center for ESD Protection Designs. His research covers Analog/Mixed-Signal/RF ICs, Integrated Design-for-Reliability, 3D Heterogeneous Integration, IC CAD and Modelling, Nano Devices and Circuits, and LED Visible Light Communications. Wang received the CAREER Award from the National Science Foundation. He published one book and 240 papers, and holds 13 US patents. Wang was editor for IEEE Electron Device Letters, IEEE Transactions on Circuits and Systems I & II, IEEE Journal of Solid-State Circuits and IEEE Transactions on Electron Devices. He has been an IEEE Distinguished Lecturer for IEEE Electron Devices Society, IEEE Solid-State Circuits Society and IEEE Circuits and Systems Society. He is Jr. Past President and was President (2014-2015) of IEEE Electron Devices Society. He was Chair of the IEEE CAS Analog Signal Processing Technical Committee (ASPTC) and committee member for the SIA International Technology Roadmap for Semiconductor (ITRS). He is IEEE 5G Initiative member. He was General Chair for IEEE RFIC Symposium (2016) and served as committee member for many IEEE conferences, including IEDM, EDTM, BCTM, ASICON, IEDST, ICSICT, CICC, RFIC, APC-CAS, ASP-DAC, ISCAS, IPFA, ICEMAC, NewCAS, ISTC, IRPS, AP-RASC, MAPE, EDSSC, MIEL, etc. He is an IEEE Fellow and AAAS Fellow.

6. Beamforming and Receiver Circuits

Friday 9:50 AM - Bay View Ballroom
Session Chair: Leonardo Vera
Co-chair: Dietmar Kissinger

(6.1) 9:50 AM - 10:40 AM - Toward Efficient, Reconfigurable, and Compact Beamforming for 5G Millimeter-Wave Systems (Invited)

Brian Floyd, Anirban Sarkar, Kevin Greene, and Yi-Shin Yeh
In this work, we present circuits and architectures for efficient, reconfigurable and compact beamforming. First, we present techniques to improve peak and back-off power-added efficiency (PAE) of SiGe power amplifiers, demonstrated with a 28-GHz harmonic-tuned amplifier (+15.5 dBm output 1-dB compression point, 35% peak PAE, 11.5% PAE at 6-dB back-off) and a 60-GHz Doherty amplifier (+17.1 dBm output 1-dB compression point, 23.7% peak PAE, 13% PAE at 6-dB back-off). Second, we present a dual-vector Doherty beamformer architecture which allows reconfiguration between an efficient Doherty mode and a linear class-AB mode, demonstrated in SiGe at 60 GHz (+16.7 dBm output 1-dB compression point and 7% PAE at 6-dB back-off). Finally, we present a compact architecture for beamformers which features dual-vector scaling functions within each element and then global combining and interpolation. This is demonstrated with a 28-GHz dual-vector receiver array in SiGe which uses only 0.3 mm² for each receiver front-end.

(6.2) 10:40 AM - 11:05 AM - A 28 GHz Transceiver Chip for 5G Beamforming Data Links in SiGe BiCMOS
Kerim Kibaroglu, Mustafa Sayginer, and Gabriel M. Rebeiz
This paper presents a 28-32 GHz transceiver chip architecture in SiGe BiCMOS to meet the requirements of 5G phased-array communication links. An asymmetric design is employed for the transmit and receive paths to deliver an output P1dB of 8 dBm in TX mode and to achieve an input P1dB of 0 dBm in RX mode. The chip can operate with an external LO at 10-16 GHz and 20-28 GHz with the use of an on-chip doubler option. All switches on RF, LO and IF paths are implemented using SiGe HBTs for low loss and wideband operation. An on-chip elliptic filter is implemented in the TX path to reject the upconverted image and LO leakage to meet spectral mask requirements. The chip was tested in the TX mode with an 802.11ad MCS-10 waveform and achieves 3.9% EVM at 3 Gbps physical rate.

(6.3) 11:05 AM - 11:30 AM - A 32.8 dB gain, 3.54 dB NF, 7 mW, 20.35 GHz LNA with embedded 30 GHz band-stop filter
Filipe Tabarani and Hermann Schumacher
This paper presents a 20.35 GHz low power, high gain, low-noise amplifier (LNA) with a 30 GHz band-stop filter embedded in the matching network. Designed in a 0.25 µm SiGe:C BiCMOS technology, it meets the specifications imposed by a full-duplex K/Ka-band shared aperture active phased-array antennas for satellite communications. The LNA exhibits a measured gain of 32.8 dB at 20.35 GHz and a 3 dB bandwidth of 2.25 GHz. The measured IIP3, IP1dB, and OP1dB are -21.2, -34.3 and -2.5 dBm, respectively. Including the losses due to the band-stop filter and the bondwire interconnects between chip and board, it achieves 3.54 dB NF at the center frequency. Among published K-band counterparts in Silicon technologies, the LNA has the highest gain and the best figure of merit, considering noise, gain, and linearity. It consumes only 7 mW, with a chip area of 407 x 287 µm².

(6.4) 11:30 AM - 11:30 AM - A Low-Power 120-GHz Integrated Sixport Receiver Front-End with Digital Adjustable Gain in a 130-nm BiCMOS Technology
Matthias Voelkel, Hartmut Hirsch, Marco Dietz, Robert Weigel, Amelie Hagelauer, and Dietmar Kissinger
In this paper a 120 GHz monolithic low-power sixport receiver front-end including two variable gain amplifiers, a passive sixport network, four detectors and a digital serial interface (SPI) is presented. The measurement principle is based on the additive superposition of two incident millimeter-wave signals, whereas the superposition must be fulfilled under special conditions. After power detection, the quadrature components can be extracted. The proposed measurement system is well suited for industrial radar applications, as well as for biomedical applications and it is further more well suited for communication systems. The receiver has been designed using a 0.13 µm SiGe BiCMOS process from IHP (SG13G2). The whole integrated circuit has a size of 1560 µm x 900 µm and only consumes 102.3 mW from a 3.3 V supply. The receiver exhibits a 1 dB compression point of -13 dBm at the center frequency. The bandwidth is 15.5 GHz and covers the lower

part of the D-Band. The gain of the input amplifier can be adjusted from 3 to 16 dB by a digital interface. The maximum power consumption of the VGA is 46.2 mW.

7. Lost in Modeling?

Friday 9:50 AM - Watson Island
Session Chair: Michael Schroter
Co-chair: Sadayuki Yoshitomi

(7.1) 9:50 AM - 10:15 AM - Evaluation of the impact of the external collector resistance on results from parameter scaling for heterojunction bipolar transistors
Andreas Pawlak and Michael Schröter
It is demonstrated that the external collector resistance, representing the voltage drop from the collector terminal to the internal collector node, and the corresponding time constant can have a large impact on the extraction of geometry scalable compact model parameters for bipolar transistors. Furthermore, the accuracy of two widely used extraction methods is evaluated based on data obtained from 2D numerical device simulation and a compact model for transistors with different emitter widths.

(7.2) 10:15 AM - 10:40 AM - A Tunable Bipolar: Investigation of effects and a MEXTRAM based VerilogA model adaptation of Field Effect Electrode influenced High Voltage SiGe HBTs
Breandán Ó hAnnaidh
This paper presents a Verilog-A compact model adaptation for a High Voltage SiGe HBT in a DTI on SOI process incorporating characteristic changes observed from a Field Effect Electrode. The output characteristics of the Bipolar are controlled, or 'tuned', by what is effectively an additional terminal. The model proposed is based on MEXTRAM and includes a new terminal node. The main additional effects are captured through the use of empirical formulae, while maintaining the bulk of the original code. The model is validated against DC and AC results from on-wafer Si test structures.

(7.3) 10:40 AM - 11:05 AM - Extracting the Temperature Dependence of Thermal Resistance from Temperature-Controlled DC Measurements of SiGe HBTs
Suresh Balanethiram, Jorg Berkner, Rosario D'Esposito, Sebastien Fregonese, Didier Celi, and Thomas Zimmer
In this paper, we study and analyze the existing techniques in literature to extract the self-heating thermal resistance from the measured DC electrical behaviour of silicon-germanium heterojunction bipolar transistors (SiGe HBTs) focusing their dependence on device junction temperature and propose a simple extraction technique that shows superior accuracy than the existing extraction methodologies. Our approach is scalable and validated with model card simulations across different emitter geometries for a wide temperature range. We also present the applicability of our approach on measured data of a SiGe HBT fabricated in STMicroelectronics B55 process.

(7.4) 11:05 AM - 11:30 AM - Silicon Modelers Are from Mars, GaAs Modelers are from Venus (Invited)
Peter Zampardi
~~Men~~ Silicon Modelers Are from Mars, ~~Women~~ GaAs Modelers Are from Venus is a ~~book written by The book~~ paper that states that most common ~~relationship~~ modeling differences ~~problems~~ between ~~men~~ silicon and ~~women~~ are a result of fundamental ~~psychological~~ philosophical differences between the ~~sexes~~ modelers and process users, which the author exemplifies by means of its eponymous metaphor: that ~~men~~ silicon and ~~women~~ GaAs modelers are from distinct planets—~~men~~ silicon modelers from Mars and ~~women~~ GaAs modelers from Venus—and that each ~~sex~~ group is acclimated to its own ~~planet's~~ technology's society and customs, but not to those of the other. One example is ~~men's~~ silicon modelers complaint that if they offer solutions to problems that ~~women~~ GaAs modelers bring up in conversation, the GaAs modelers are not necessarily interested in solving those problems, but mainly want to talk about them. The ~~book~~ paper asserts each ~~sex~~

groups can be understood in terms of distinct ways they respond to customer expectations ~~stress~~ and ~~stressful situations~~ the products their models are used to design. The focus is on bipolar modeling in SiGe and GaAs technologies.

8. Optical Communications Circuits

Friday 1:00 PM - Bay View Ballroom
Session Chair: Johann-Christoph Scheytt
Co-chair: Kimia T. Ansari

(8.1) 1:00 PM - 1:25 PM - A 100 Gbit/s 2 Vpp Power Multiplexer in SiGe BiCMOS Technology for Directly Driving a Monolithically Integrated Plasmonic MZM in a Silicon Photonics Transmitter
Christopher Uhl, Horst Hettrich, and Michael Möller
An 8:1 multiplexer with a power output stage (PMUX) in SiGe BiCMOS technology for directly driving a plasmonic Mach-Zehnder modulator (MZM) with a 2 Vpp differential voltage swing at a data rate of 100 Gbit/s is presented. The PMUX is intended to be monolithically integrated with an ultrashort MZM on a single chip in a novel silicon photonic process. Through this integration, the bandwidth and output voltage swing could be improved compared to an external MZM load that requires far end termination. Furthermore, the direct driving by the PMUX eliminates the traditional driver amplifier, whereby power can be saved and the signal quality can be improved. Electrical measurements of the MUX show clear eye openings at 100 Gbit/s up to a 2.0 Vpp differential output voltage swing at an external 50 Ohm oscilloscope load. The inherent high-speed capability of the PMUX is demonstrated at the speed limit of the available measurement equipment at 140 Gbit/s, where the PMUX still achieves 1.2 Vpp differential voltage swing, which is a record for SiGe bipolar technology.

(8.2) 1:25 PM - 1:50 PM - Fully-differential, DC-coupled, Self-biased, Monolithically-integrated Optical Receiver in 0.25µm Photonic BiCMOS Technology for Multi-Channel Fiber Links
Sergiy Gudyriev, J. Christoph Scheytt, Lei Yan, Christian Meuer, and Lars Zimmermann
A fully-differential receiver structure for fiber links is presented, in which the photodiode (PD) is DC-coupled to the transimpedance amplifier (TIA) and biased through the feedback resistors. The biasing voltage is defined by the internal structure of the input stage. Different options are suggested that allow to adjust PD biasing. Multiple architecture variants are proposed, that were implemented in 0.25µm SiGe BiCMOS technology. Initial measurement results are reported, proving the feasibility of the concept. 40Gbps data rate was achieved by monolithically integrated optical receiver that consumes 120mW of power from a single 3.3V power supply. A 25Gbps hybrid receiver designed to comply with a specific standard is also presented, featuring large horizontal eye opening of 800mV, OMA of -15dBm at BER of 10^{-6} and power dissipation of 330mW from a single 3.3V power supply.

(8.3) 1:50 PM - 2:15 PM - A 60 GHz Bandwidth Differential Linear TIA in 130 nm SiGe:C BiCMOS with < 5.5 pA/sqrt(Hz)
Iria Garcia Lopez, Ahmed Awny, Pedro Rito, Minsu Ko, Ahmet Cagri Ulusoy, and Dietmar Kissinger
A differential linear TIA implemented in a 130 nm SiGe:C BiCMOS technology with ft/fmax/BVCEO of 300 GHz/500 GHz/1.7 V is presented. It features a bandwidth of 60 GHz, 62.5 dBOhm differential transimpedance gain and 5.46 pA/sqrt(Hz) averaged input-referred current noise density, while dissipating 85 mW of DC power. The measured THD is better than 3% for 500 mVppd output swing and input current of 400 µApp. Clear NRZ eye diagrams up to 56 Gb/s, as well as PAM-4 eye diagrams up to 30 GBd (both setup limited) are also reported. To the author's best knowledge, this design exhibits record low-noise performance among > 50 Gb/s-class silicon-based broadband TIAs towards 100/400 Gb/s optical links.

(8.4) 2:15 PM - 2:40 PM - A wideband square-law power detector with high dynamic range and combined logarithmic amplifier for 100 GHz F-Band in 130 nm SiGe BiCMOS

Paul Stärke, Vincent Rieß, David Fritsche, Corrado Carta, and Frank Ellinger
This work presents an active wideband power detector, operating between 90 GHz and 140 GHz. The topology is a low-biased bipolar cascode with a diode-connected pMOS transistor as non-linear load for extending the quadratic characteristic. To realize a linear-in-db behavior a low-power logarithmic amplifier with offset compensation is directly coupled to the power detector. The circuit is implemented in 130 nm SiGe BiCMOS. The achieved dynamic range of the square-law region is 38 dB, with a total dynamic range of 48 dB and a minimum input level of below -50 dBm. The static power consumption of the detector and logarithmic amplifier is 68 µW and 400 ÂµW.

9. Boosting Device Performance

Friday 1:00 PM - Watson Island
Session Chair: Vibhor Jain
Co-chair: Kai Kwok

(9.1) 1:00 PM - 1:25 PM - Predicting Hard Failures and Maximum Usable Range of SiGe HBTs
Rafael Perez Martinez, Uppili S. Raghunathan, Anup P. Omprakash, Brian R. Wier, Michael A. Oakley, Zachary E. Fleetwood, and John D. Cressler
This paper presents an overview of the various failure mechanisms observed as a SiGe HBT is operated outside of traditionally defined electrothermal safe operating areas (SOAs). The concepts of hard and soft safe operating area (SOA) boundaries are defined in this work. This provides two different viewpoints which determine the degradation and failure of a SiGe HBT as a function of bias conditions. Measurements were performed on state-of-the-art SiGe HBTs to measure the hard SOA boundaries in terms of physical parameters such as geometry, layout configuration, and temperature. The outcome of this work can serve as the stepping-stone to a "red flag" warning mechanism for the detection of hard SOA boundaries within a circuit design environment.

(9.2) 1:25 PM - 1:50 PM - Enhanced Bipolar Transistor Design for the Linearization of the Base-Collector Capacitance
Jordi vd Meulen and Leo de Vreede
A frequency, bias and output power independent linearization technique for reducing the non-linear base-collector capacitance related distortion is proposed. Based on Volterra series analysis, the optimum base-collector capacitance for linear device operation is determined while respecting physical constrains. It is shown that by modifying the extrinsic base-collector region for an otherwise uncompromised device, the Cbc linearity compensation can be included within the transistor design itself. The practicality of this implementation is demonstrated by considering the doping profile accuracy requirements for achieving a significant OIP3 improvement of at least 5dB.

(9.3) 1:50 PM - 2:15 PM - Improving the Horizontal Current Bipolar Transistor Breakdown Voltage by Floating Field Plates
Marko Koricic, Josip Zilak, and Tomislav Suligoj
A method for improvement of breakdown voltage of the Horizontal Current Bipolar Transistor (HCBT) by application of floating field plates (FFPs) is presented. The FFPs are used for shaping of the potential distribution and the electric field in the base-collector depletion region. The BVCEO improvement from 13 V to 25 V by the addition of one FFP to a double-emitter HCBT is demonstrated by measurements of fabricated devices. The FFP is fabricated by the extrinsic base implantation and is aligned to the extrinsic base, allowing for ideal control of the electric field shaping. New structure is added to the HCBT BiCMOS process flow at zero-cost. Simulations show that multiple FFPs can be used for the increase of the BVCEO in discrete steps. BVCEO of 44 V is achieved by using 5 FFPs.

(9.4) 2:15 PM - 2:40 PM - Physics-based modeling of SiGe HBTs with fT of 450 GHz with HICUM Level 2
Andreas Pawlak, Bernd Heinemann, and Michael Schröter

SiGe HBT technologies have increasingly seen improvements in their maximum operating speed. These are attributed to aggressive vertical and lateral device scaling. While the latter is generally captured by scaling equations for model parameters, physical effects caused by the former need to be described by the model equations. Examples for effects that gain importance with shrinking device dimensions are the impact of quasi-ballistic transport in the base and non-local effects in the collector of the transistor. This paper shows the application of HICUM/L2 to the latest generation of very highspeed SiGe HBTs and demonstrates the accurate modeling of the important device characteristics as well as the possibility to extract the parameters of the corresponding 1D transistor.

10. Conversion Circuits

Friday 3:00 PM - Bay View Ballroom
Session Chair: Michael Möller
Co-chair: Koichi Murata

(10.1) 3:00 PM - 3:25 PM - A 40 GS/s 4 bit SiGe BiCMOS Flash ADC
Xuan-Quang Du, Markus Grözing, Matthias Buck, and Manfred Berroth
This paper presents the design and experimental test of a 40 GS/s 4 bit single-core flash ADC in a 0.13 µm SiGe BiCMOS technology. The ADC exploits a traveling-wave concept and integrates a new low-complexity Pseudo-XOR gray encoder that makes use of folded-cascode differential logic. Up to a sampling rate of 39.04 GS/s the ADC provides a measured ENOB of more than 3 bits and a SFDR of more than 24.8 dBc within the frequency band from DC to 20 GHz. At 40.32 GS/s the frequency band for a minimum effective resolution of 3 bits is 12 GHz and at 42.24 GS/s it is about 5.3 GHz.

(10.2) 3:25 PM - 3:50 PM - A Linear Active Combiner Enabling an Interleaved 200 GS/s DAC with 44 GHz Analog Bandwidth
Horst Hettrich, Rolf Schmid, Lars Altenhain, Johann Würtele, and Michael Möller
A linear active combiner with an analog bandwidth of 50 GHz is presented. It is well suited for interleaving the outputs of two digital-to-analog converters (DACs), because it features almost identical forward transmission of both channels and good isolation between the inputs. Featuring a high linearity it can generate output signals up to 1.6 Vpp differential voltage swing with an effective number of bits (ENoB) of 6. The performance of the combiner is demonstrated by characterization of the standalone device and in a time interleaved DAC setup where a sampling rate of 200 GS/s with an analog bandwidth of 44 GHz and an ENoB of > 4.5 is achieved.

(10.3) 3:50 PM - 4:15 PM - A SiGe-HBT 2:1 Analog Multiplexer with more than 67 GHz Bandwidth
Tobias Tannert, Xuan-Quang Du, Daniel Widmann, Markus Grözing, Manfred Berroth, Christian Schmidt, Christoph Caspar, Jung Han Choi, Volker Jungnickel, and Ronald Freund
This paper presents a 2:1 Analog Multiplexer (AMUX) in a SiGe-HBT technology. The AMUX is used for time interleaving operation of two digital-to-analog converters (DACs) and therefore extends both the sampling rate and the bandwidth compared to a single DAC. The linear AMUX signal path allows for generation of broadband signals with higher order modulation schemes which is essential for raising data rates in optical communication networks. The AMUX provides a differential peak-to-peak output voltage of up to 1 V with linear gain. A signal path 3-dB bandwidth exceeding 67 GHz has been measured. The clock path exhibits a 3-dB bandwidth of 60 GHz. S-parameter measurements are presented. Measured PAM4 eye diagrams at 56 GS/s from the time interleaving operation of two DACs are reported.

11. Millimeter-Wave VCOs and Signal Generation

Friday 3:00 PM - Watson Island
Session Chair: Wibo Van Noort
Co-chair: Hua Wang

(11.1) 3:00 PM - 3:25 PM - A K-Band Low-Noise Bipolar Class-C VCO For 5G Backhaul Systems in 55nm BiCMOS Technology
Niccolò Lacaita, Matteo Bassi, Andrea Mazzanti, and Francesco Svelto
The development of 5G communication systems is underway. When employing 64 QAM, very low phase noise levels are required to limit EVM - i.e. less than -117dBc/Hz at 1MHz offset from f=20GHz. In this paper, the challenges of achieving such a low phase noise are discussed in detail. The choice between CMOS vs BJT devices is investigated and the impact of the base resistance intrinsic in BJT-based VCOs is addressed. BJT-based VCO shows ~2dB better phase noise when compared to CMOS-based VCO and low supply is employed. When higher supply is leveraged, BJT-based VCO advantage is kept while CMOS-based VCO is not able to reach the targeted tuning range due to thick-oxide devices parasitics. Emphasis is on the minimization of L/Q inductor versus quality factor ratio, to further minimize phase noise. Prototypes in a 55nm BiCMOS technology were operated at 2.5V supply with the largest amplitude allowed by reliability constraints. Measurements show a phase noise as low as 119dBc/Hz at 1MHz from a 20GHz carrier offset with a tuning range (TR) of 19% and FoM=-187dBc/Hz. Power consumption is 56mW. To the best of authors' knowledge, the presented VCO shows the lowest reported phase noise among state-of-the-art BiCMOS VCOs with TR>10%.

(11.2) 3:25 PM - 3:50 PM - A Multi-Phase Clock Coulpled VCO Using Dual-Tank Magnetic Coupling Technique
Rong Jiang, Rong Jiang, Hossein Noori, and Fa Dai
This paper presents a novel coupled-oscillator RFIC for multi-phase clock generation. The design achieves low phase noise while maintaining strong coupling among oscillator cores. The proposed transformer-based dual-tank topology forms a loop of coupling path for enhanced multi-phase coupling. The phase noise optimization is accomplished by leveraging the dual-tank and the adaptive-biasing feedback techniques, while the transformers facilitate strong magnetic coupling among oscillator cores. Full electro-magnetic (EM) modeling of all transformers and the passive interconnecting routes has been performed using EMX in order to ensure that simulated performance reflects measurement environment. The prototype of the proposed circuit with 8 phases is implemented in a 60nm CMOS RF SOI technology. The measured phase noise is -124.3 dBc/Hz @ 1MHz offset from 2.41 GHz with 7mw power consumption for each core, and the operating frequency can be digitally tuned from 1.81GHz to 2.41 GHz.

(11.3) 3:50 PM - 4:15 PM - A Wideband 129-171 GHz Frequency Quadrupler Using a Stacked Bootstrapped Gilbert Cell in 0.13 um SiGe BiCMOS
Maciej Kucharski, Andrea Malignaggi, Dietmar Kissinger, and Herman Ng
This paper presents a wideband fully differential 129-171 GHz frequency quadrupler (FQ) based on stacked double bootstrapped Gilbert cell. The chip was fabricated in 130 nm SiGe BiCMOS technology offering heterojunction bipolar transistors (HBT) with fT /fmax of 300/500 GHz. The FQ consists of two stacked mixing stages resulting in a simple and compact circuit which occupies only 0.08 mm². A bootstrapping technique was used in order to enhance the conversion gain and improve the input matching. The FQ achieves 5 dB peak conversion gain and 2.2 dBm output power. The circuit draws a maximum current of 100 mA from 4.4 V supply. The presented frequency quadrupler is suitable to be used as a LO generation circuit for a 158 GHz radar transceiver (TRX).

(11.4) 4:15 PM - 4:40 PM - A Very Low Phase-Noise Ku-band Coupled VCO in 0.25 µm SiGe:C BiCMOS Technology With Low Frequency Pushing
David Cordeau, Jérémy Hyvert, David Cordeau, and Jean-Marie Paillot
This paper presents a fully integrated Ku-band coupled Voltage Controlled Oscillator (VCO) with very low phase noise performances, implemented in the QUBiC4X 0.25 µm SiGe:C BiCMOS process of NXP semiconductors. The originality of this design consists in using two coupled VCOs with a new bias circuit to improve the pushing and the phase noise. Under 5 V supply voltage and a maximum total power

dissipation of 231.5 mW, the proposed VCO features a phase noise of -121.4 dBc/Hz at 1 MHz frequency offset. The VCO is tuned from 13.53 GHz to 14.79 GHz with a tuning voltage varying from 1 V to 4.5 V and occupies 0.84x1.85 mm².

(11.5) 4:40 PM - 5:05 PM - A 61 GHz SiGe Transmitter Chip for Energy and Data Transmission of Passive RFID-Single-Chip-Tags with Integrated Antennas

Christian Bredendiek, Benedikt Welp, Klaus Aufinger, and Nils Pohl

This paper presents a SiGe-transmitter chip for short-range devices in the 61 GHz ISM frequency band. The presented transmitter consists of a fundamental VCO, a PA, lumped element Wilkinson-Dividers and a static divide-by-16 chain for stabilization in a PLL. Two variants of the transmitter are fabricated with supply voltages of 3.3 V and 5 V in a modern 130nm SiGe BiCMOS technology with HBTs offering an fT of 250 GHz and fmax of 370 GHz. The main goal of this work is to achieve an efficient signal source to supply a passive RFID-Tag with the maximum allowed 20 dBm EIRP for short range devices. The transmitter chips achieve a peak output power of 17 dBm, PAEPA of 18.8% and DC-to-RF efficiency of 12.9% (excluding the divider). At 61 GHz a phase noise of -102 dBc/Hz is achieved. The power consumption for the chips are 710 mW and 482 mW for the 5 V and 3.3 V variant, respectively.

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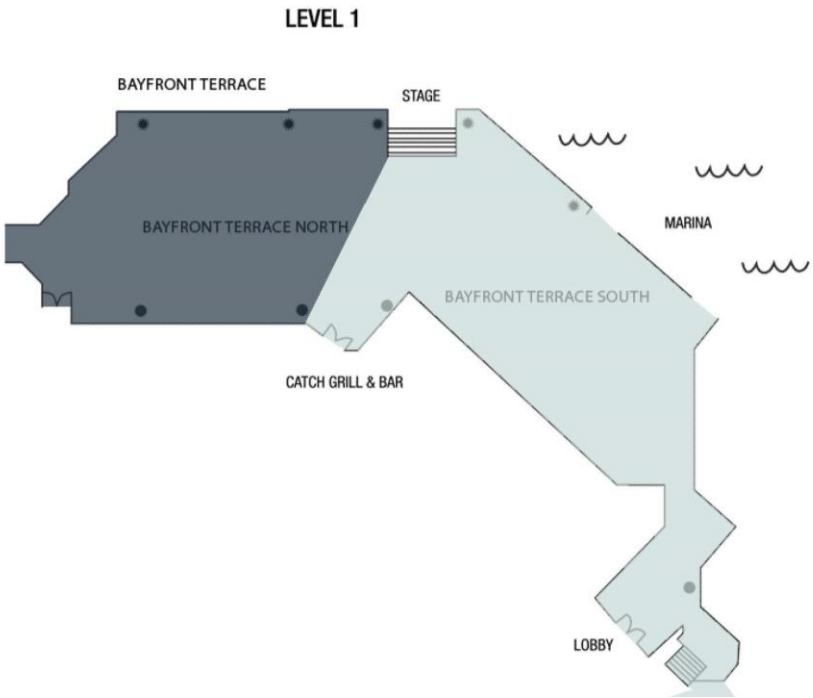
Miami Marriott Biscayne Bay

Second Floor: All conference meeting sessions will be held on the 2nd Floor.

= General Session / Breakout Room / Meals

= Breakout Room **= Registration Desk**

First Floor: Hotel lobby & restaurant



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- South Beach / Art Deco District
- Bayside Marketplace
- American Airlines Arena (Home of the Miami Heat)
- Port of Miami
- Coconut Grove
- Hard Rock Stadium (Home of the Miami Dolphins)
- Vizcaya Museum and Gardens

Crandon Park Beach

- Boat Tours (including Miami Everglades Airboat Tour)
- Zoo Miami
- Marlins Park
- Spa
- Golf
- Tennis
- Nightlife
- Casino
- Pool
- Land and water sports
- Jogging / walking / biking trails
- Dining

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HIGH-SPEED DIGITAL, MIXED-SIGNAL, & OPTOELECTRONIC ICS
Mixed analog/digital ICs - Digital ICs - (high-speed) DACs and ADCs - Op amps - Voltage references and regulators - Integrated filters - Sensors and actuators - Networking ICs, MUX/DEMUX, Clock and data recovery, Decision circuits, Equalizers - Optical data links, Laser and modulator drivers - High-voltage ICs - Biomedical electronics - Power Management ICs - Energy harvesting ICs - Motor controls - Analog subsystems within a VLSI chip - Packaging of high-performance ICs.

ANALOG, RF, AND MICROWAVE ICS
RF circuits and systems - Radio and transceiver subsystems - LNAs - AGCs - Mixers - Voltage controlled oscillators - Frequency synthesizers - Power amplifiers - RF switches - Noise and distortion suppression - RF Packaging - Integrated RF passives. Analog, RF, mixed-signal, power conversion and optoelectronic circuit blocks and ICs.

mm-WAVE & THZ ICS
Millimeter - wave circuits and systems - THz circuits and systems. MM-Wave switches and amplifiers. Phased-array antenna circuits

DEVICE PHYSICS:
New device physics phenomena in Si, SiGe, SiC, GaN, MOS, and III-V HBTs and FETs - Device design issues and scaling limits - Hot electron effects and reliability physics - Transport and high field phenomena - Noise - Linearity/Distortion - Novel measurement techniques - Operation in extreme environments (low and high temperatures, radiation effects), and ESD phenomena.

MODELING AND SIMULATION
Improved silicon-based BJT and HBT models and Physics-based modelling techniques - Improved III-V HBT and FET models and Physics-based modelling techniques - Parameter extraction methods and test structures - High-frequency measurement, calibration and de-embedding techniques - RF and thermal simulation techniques - Modelling of passives, interconnect and packages - Statistical modelling - Device, process and circuit simulation - CAD/modelling of power devices - packaging of power devices.

PROCESS AND DEVICE TECHNOLOGY
Device and IC manufacturing processes, testing methodologies, & reliability
Integration of III-V devices on Si, High performance devices such as GaN power conversion devices, near-THz SiGe HBTs & InP HEMTs, Novel devices such as tunnel FETs (TFETs), carbon nanotubes, MEMS, graphene & diamond transistors,
Optoelectronic and photonic devices such as optical modulators, lasers, photodetectors, and Silicon Photonics, Thermal management technologies, thermal simulation, and advanced packaging of high-power devices and ICs.

Advances in processes and device structures demonstrating high speed, low power, low noise, high current, high voltage, etc. BiCMOS processes - Advanced process techniques - Si and SiC homojunction bipolar/BiCMOS devices and SiGe heterojunction bipolar/BiCMOS devices - Manufacturing solutions related to Bipolar and BiCMOS yield improvements - Fabrication of high-performance passive components, sensors, and MEMs - Process technology related to discrete and integrated bipolar/BiCMOS power devices - IGBT, RF power devices. Wide bandgap bipolar devices (e.g., SiC) and related process technology - 3D Integration - Reliability and testing for IC manufacturing.

IMPORTANT DATES
Friday May 11, 2018 – Abstracts Due
Friday, June 22, 2018 – Decision E-mail Sent
Friday, August 3, 2018 – Final Manuscript Due

Authors must submit an abstract (not more than 4 pages including figures and other supporting material) of results not previously published or not already accepted by another conference. Papers will be selected on the basis of the abstract.

The abstract must concisely and clearly state:

a) The purpose of the work
b) What specific new results have been obtained
c) How it advances the state-of-the-art or the industry
d) References to prior state-of-the-art
e) Sub-committee preference:
   - Analog, RF, and Microwave ICs
   - Device Physics
   - High-Speed Digital, Mixed-Signal, & Optoelectronic ICs
   - Modeling & Simulation
   - mm-Wave and THz ICs
   - Process & Device Technology

Abstracts must include: title, name(s) of the authors(s), author affiliations, corresponding authors' postal and e-mail addresses, and telephone numbers. Please indicate your subcommittee preference. The committee will honor these preferences where possible, but reserves the right to place the paper in other review categories.

Company and governmental clearances must be obtained prior to submission of the abstract.

Accepted abstracts may be used for publicity purposes. Portions of these abstracts may be quoted in magazine articles publicizing the Symposium. **Please note on the abstract if this is not acceptable.**

Abstracts must be submitted electronically using the www.bcicts.org system. The **only** accepted file format is **PDF**. Authors will be informed of the decision on their submissions by June 22, 2018. Authors of accepted papers are required to submit a **PDF** of a 4-page camera-ready paper to IEEE by August 3, 2018 for publication in the Symposium Digest.

Further questions on abstract submission may be addressed to the Symposium Technical Program Co-Chairs:

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